

Q190

Rev : 1.0

TABLE OF CONTENTS

Page	Index	Page	Index
1	COVER PAGE	26	SATA HDD
2	Block Diagram	27	Card Reader RTS5229
3	Power Delivery	28	LAN RTL8111F
4	Power Sequence,Reset Diagram	29	LAN RJ45
5	GPIO Function Map	30	AUDIO ALC662
6	CPU - DMI/FDI/PEG	31	AUDIO JACK
7	CPU - MISC	32	USB3.0 Port
8	CPU - DDR3	33	USB2.0 Port
9	CPU - PWR1	34	SIO-IT8772E/FX
10	CPU - PWR2	35	FAN/LED/Thermal Sensor
11	CPU - GND	36	PWR_Adapter In
12	CPU - RESERVED	37	PWR_VHOCORE/GFX_CORE-1
13	DDR3 - SODIMM	38	PWR_VHOCORE/GFX_CORE-2
14	PCH(HDA,JTAG,SPI,SATA)	39	PWR_V5AL/V3.3AL
15	PCH(PCI-E,SMBUS,CLK)	40	PWR_+1_5V/+0_75V
16	PCH(DMI,FDI,GPIO)	41	PWR_1.05V_VCCP/1.8V
17	PCH(LVDS,DDI)	42	PWR_VCCSA
18	PCH(PCI,USB,NVRAM)	43	PWR_System
19	PCH(GPIO,VSS_NCTF,RSVD)	44	PWR_Discharge
20	PCH(POWER1/2)	45	HOLE & BOSS
21	PCH(POWER2/2)	46	History and Changelist
22	PCH - GND		
23	Display-VGA		
24	Display-HDMI		
25	MINI_PCIE WIFI		

NOTE:

Design by


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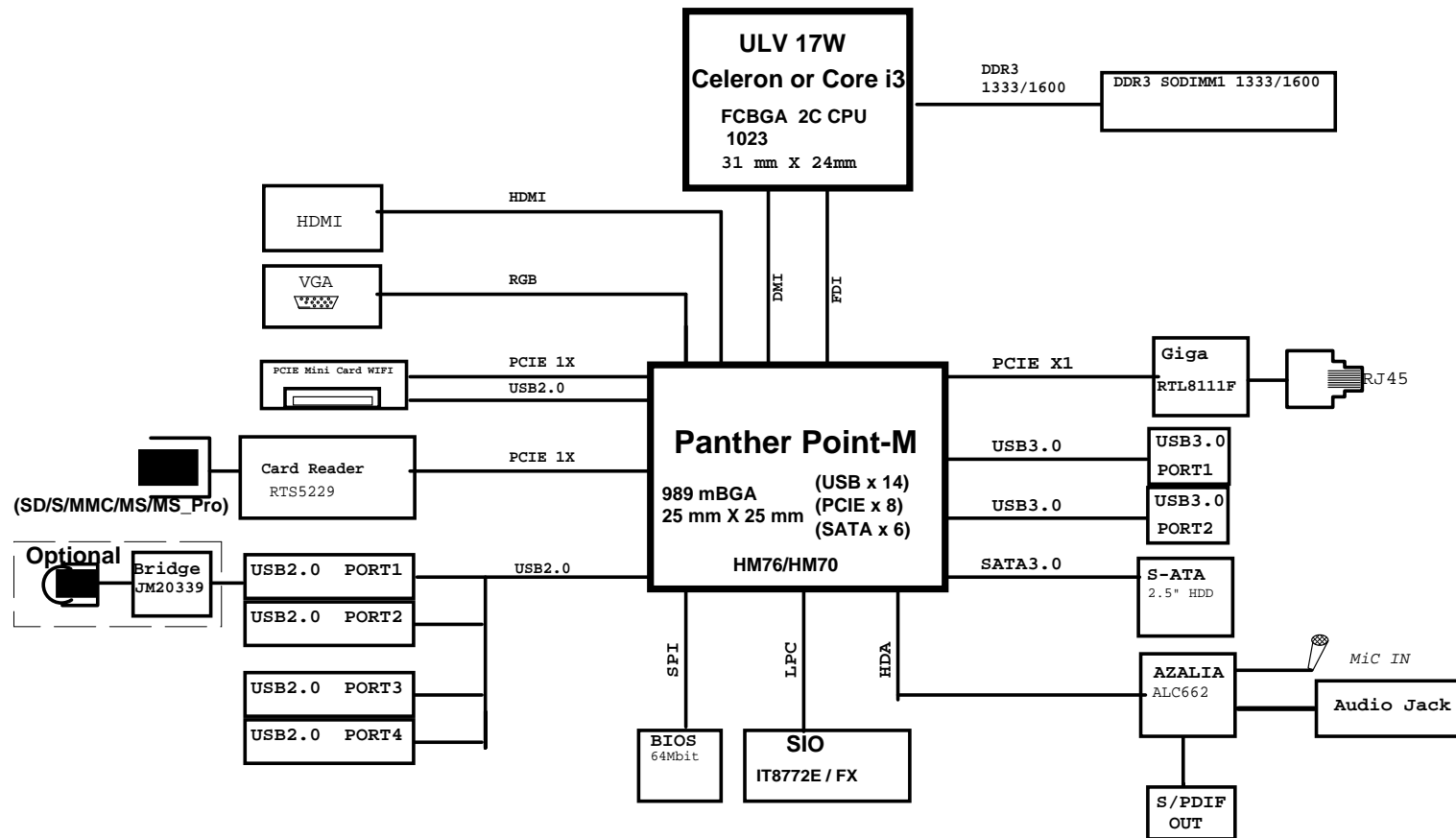
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Rev	Date	Notes
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Size Custom	Project Name BM6C66LF		Rev 1.0
Date: Sheet 1 of 46			
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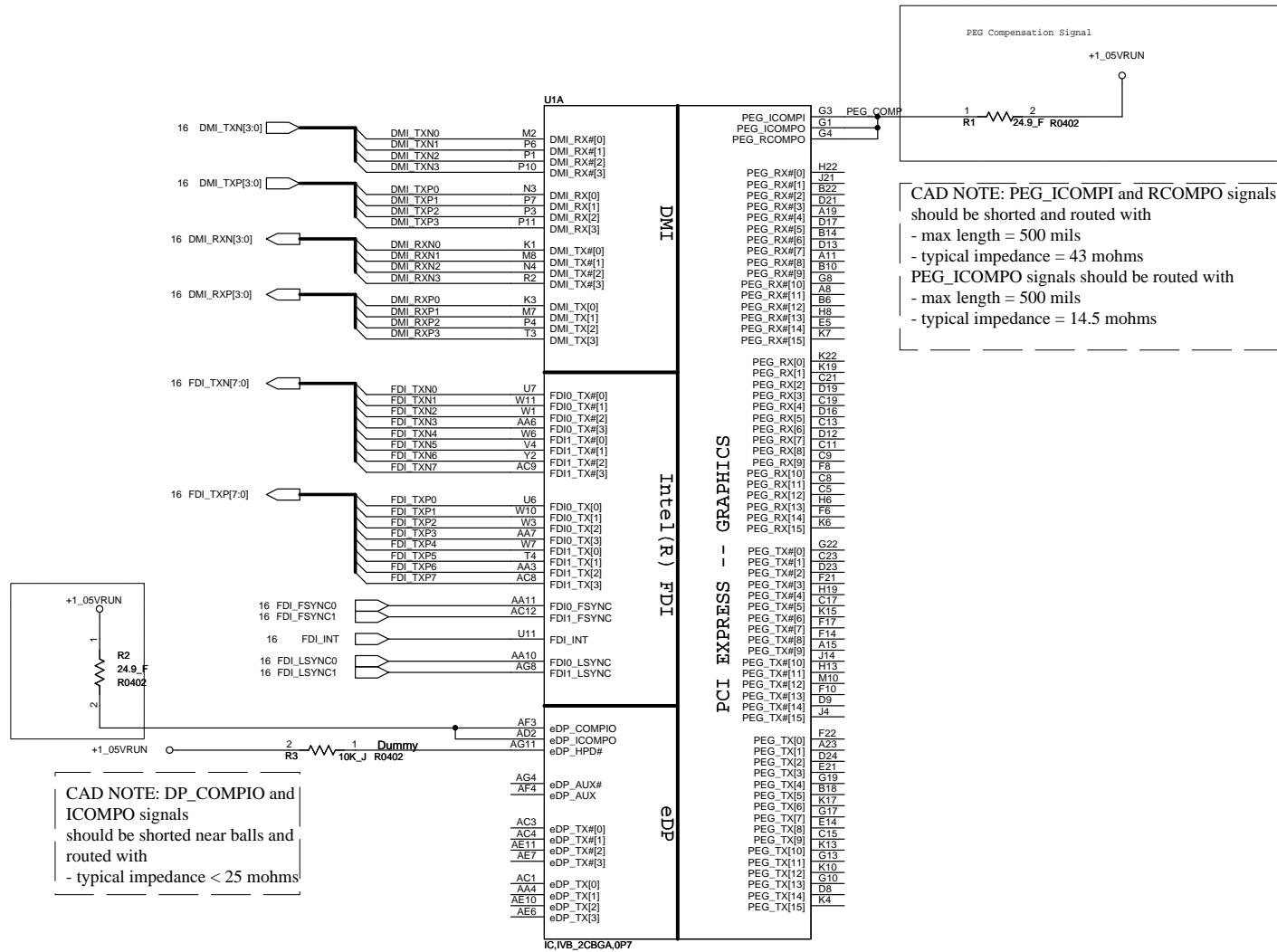
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SYSTEM BLOCK



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Page Name	BLOCK DIAGRAM		
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SANDYBRIDGE 2C BGA PROCESSOR (DMI,DP,PEG,FDI)



U1B

PROC_SELECT#

PROC_DETECT#

CATERR#

PECI

PROCHOT#

THERMTRIP#

PM_SYNC

UNCOREPWRGOOD

SM_DRAMPWROK

RESET#

IC:IVB_2CBGA,0P7

MISC

THERMAL

PWR MANAGEMENT

CLOCKS

DDR3 MISC

JTAG & BPM

BCLK

BCLK#

DPLL_REF_CLK

DPLL_REF_CLK#

SM_DRAMRST#

SM_RCOMP[0]

SM_RCOMP[1]

SM_RCOMP[2]

PRDY#

PREQ#

TCK

TMS

TRST#

TDI

TDO

DBR#

BPM#[0]

BPM#[1]

BPM#[2]

BPM#[3]

BPM#[4]

BPM#[5]

BPM#[6]

BPM#[7]

BPM#[8]

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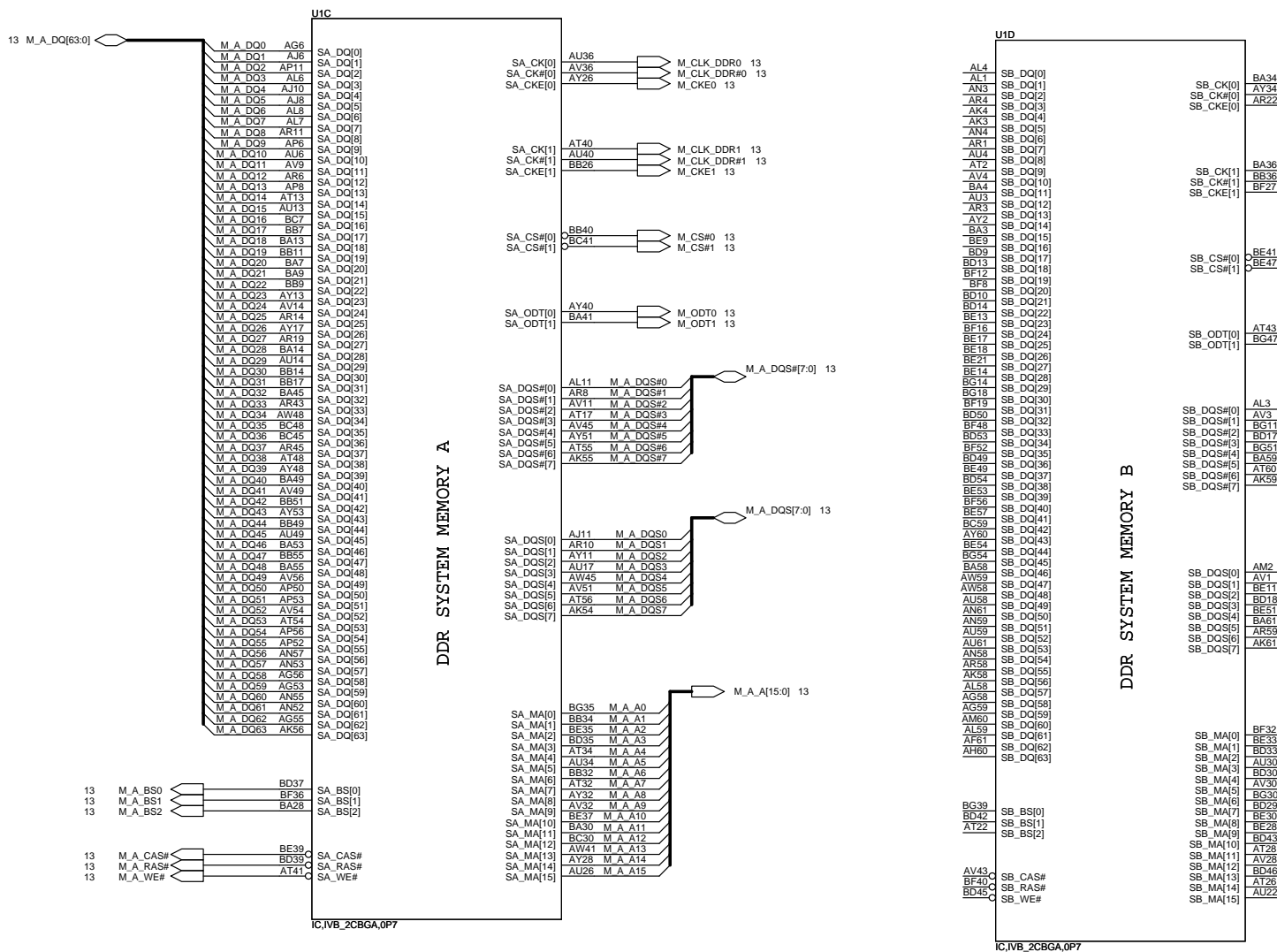
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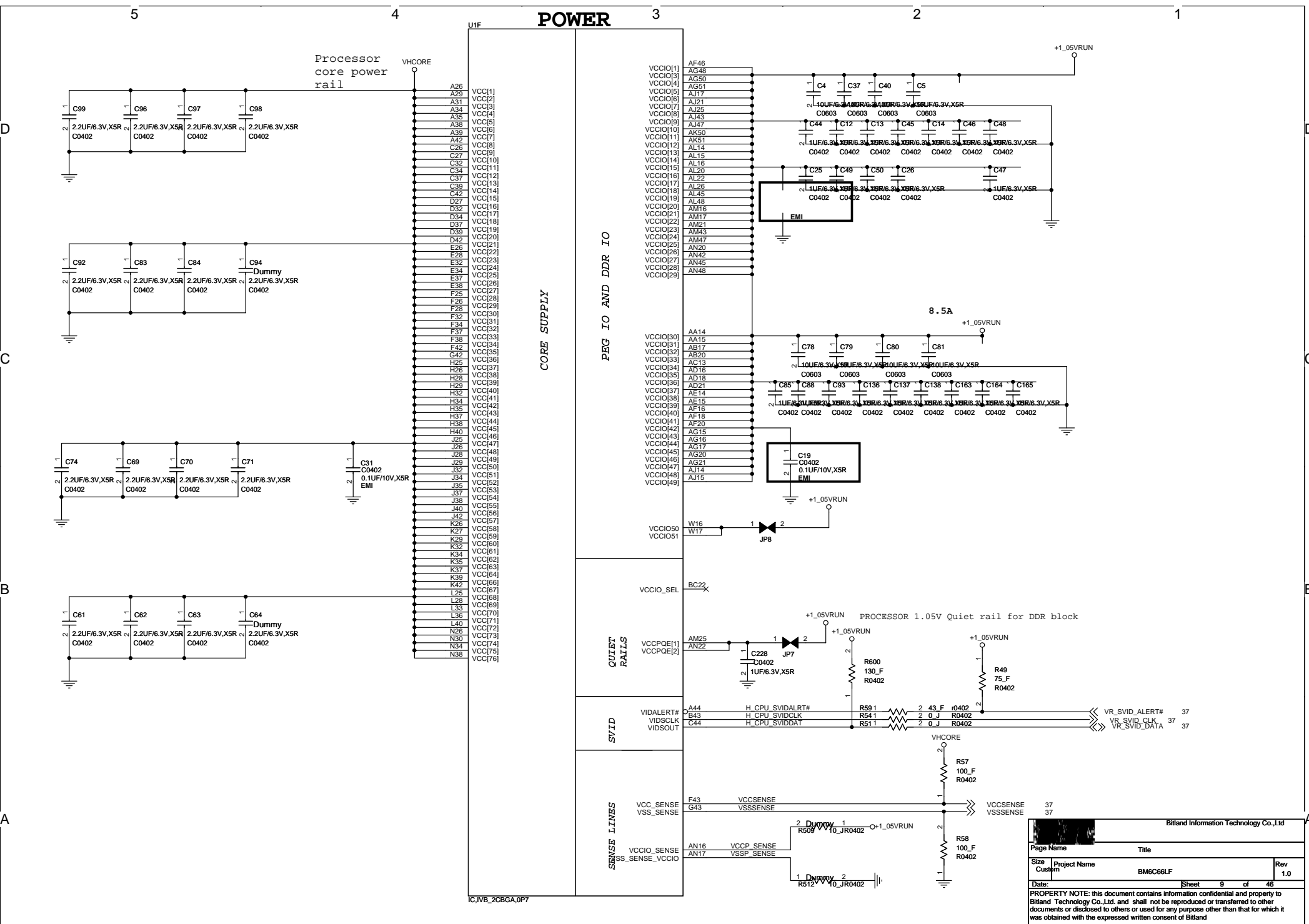
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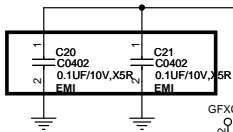
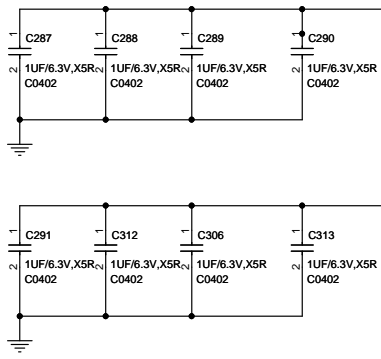
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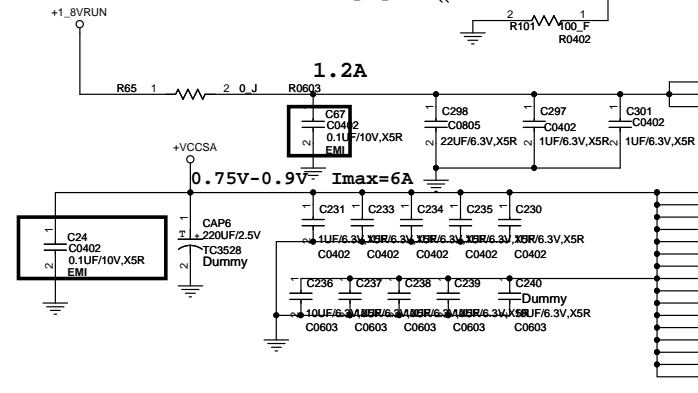


POWER

15A



1.2A



GFXCORE

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- AB47 VAXG[2]
- AB50 VAXG[3]
- AB51 VAXG[4]
- AB52 VAXG[5]
- AB53 VAXG[6]
- AB55 VAXG[7]
- AB56 VAXG[8]
- AB58 VAXG[9]
- AC51 VAXG[10]
- AD47 VAXG[11]
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- Y61 VAXG[55]
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U1G

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- Y48 VAXG[54]
- Y61 VAXG[55]
- Y61 VAXG[56]

F45

G45

VAXG_SENSE

VSSAXG_SENSE

VCCPLL[1]

VCCPLL[2]

VCCPLL[3]

VCCSA[1]

VCCSA[2]

VCCSA[3]

VCCSA[4]

VCCSA[5]

VCCSA[6]

VCCSA[7]

VCCSA[8]

VCCSA[9]

VCCSA[10]

VCCSA[11]

VCCSA[12]

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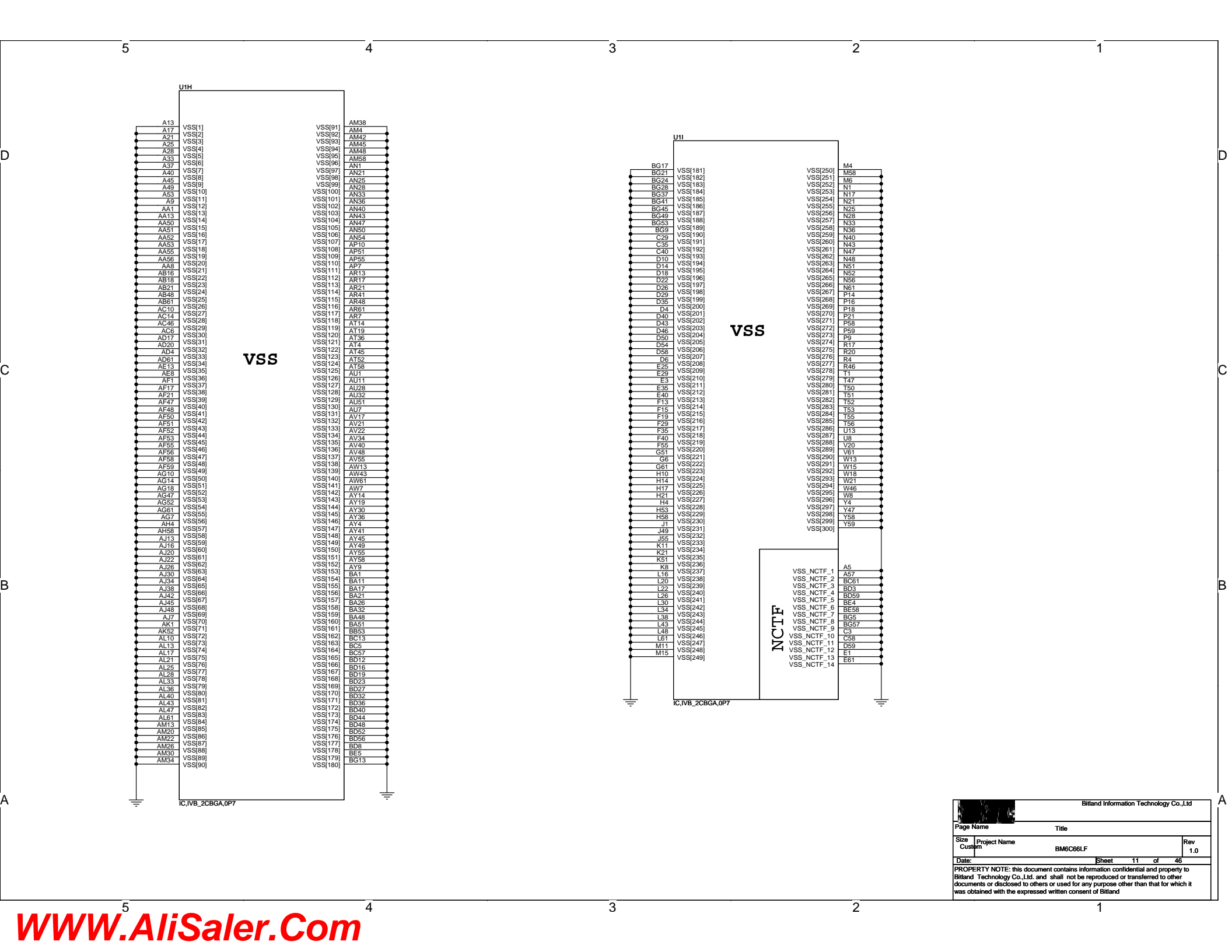
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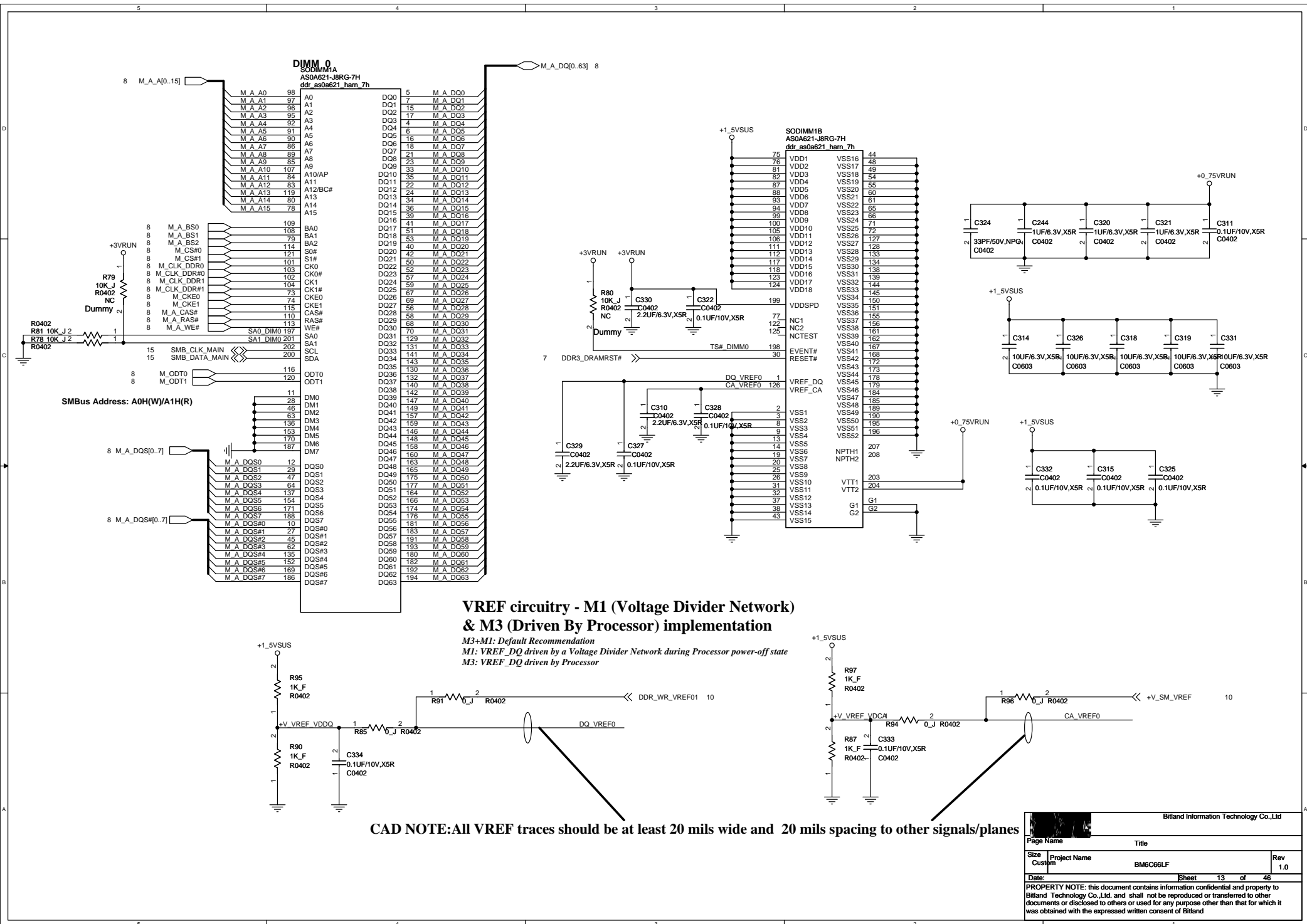
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CFG2 1:(Default) Normal Operation; Lane # definition matches socket pin map definition
CFG2 0:Lane Reversed

CFG4 1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port
CFG4 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG16: 5]
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 Function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG7 1: (Default) PEG Train immediately following xxRESETB de assertion
CFG7 0: PEG Wait for BIOS for training



D

C

B

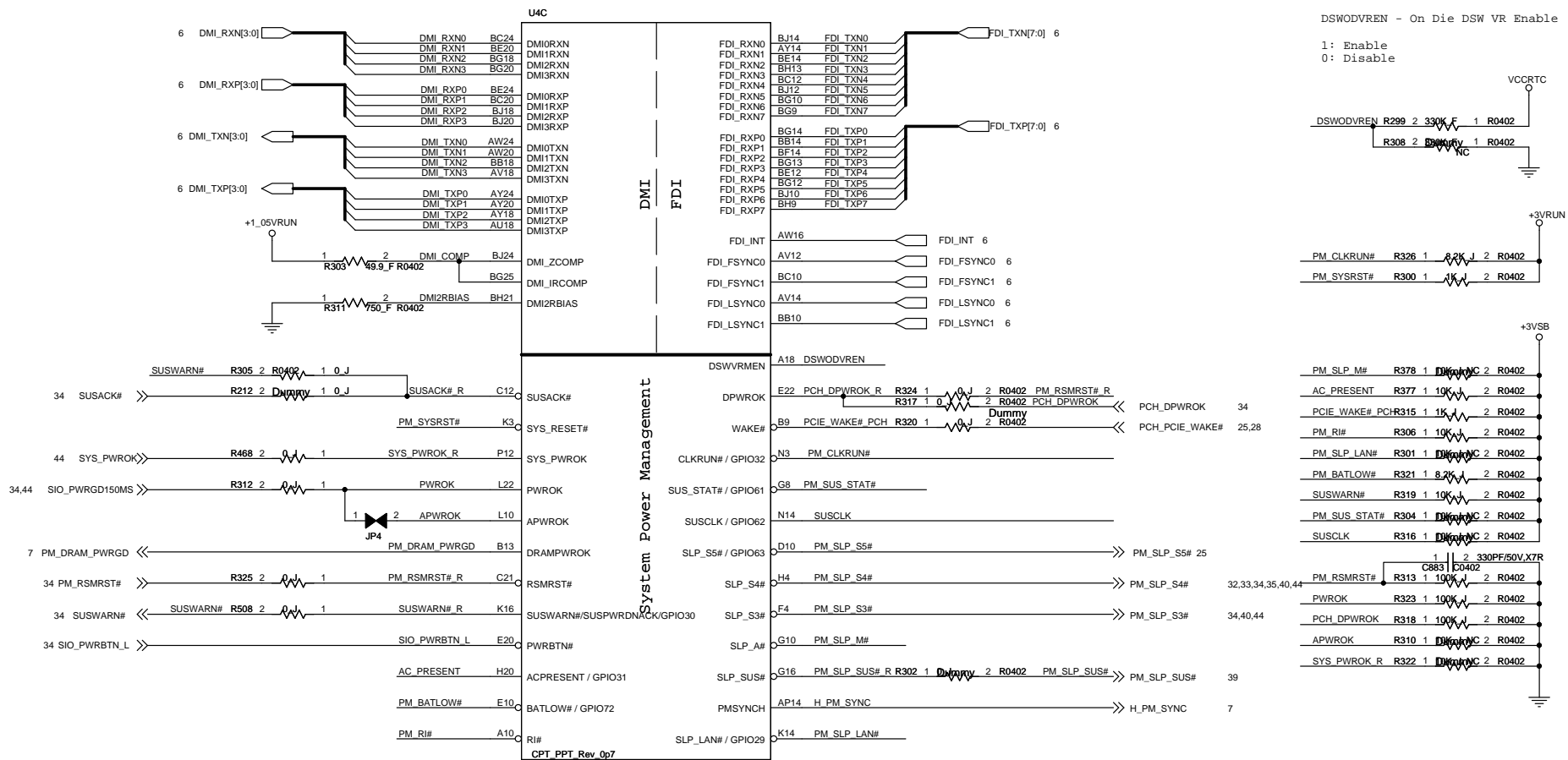
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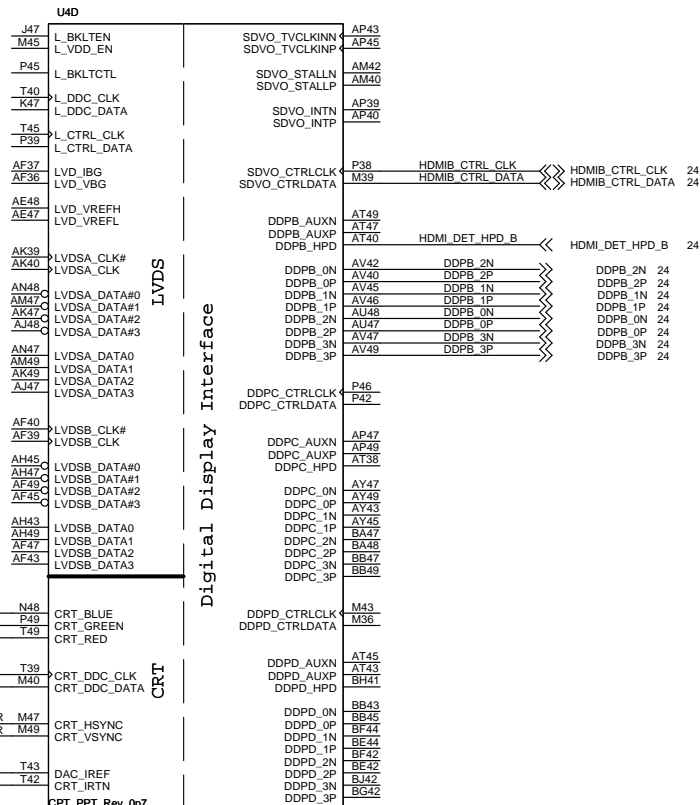
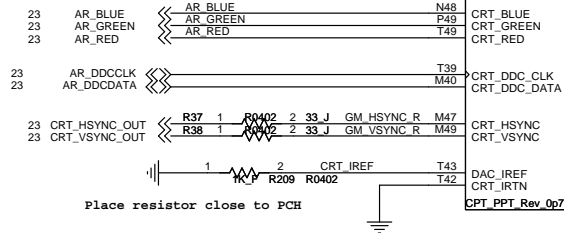
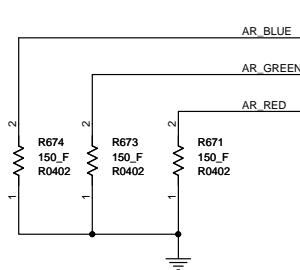
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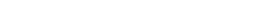
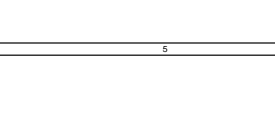
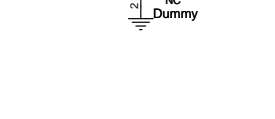
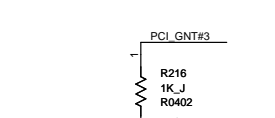
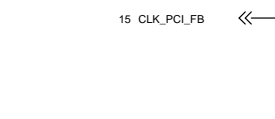
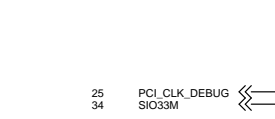
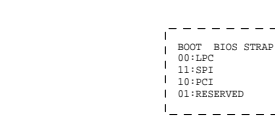
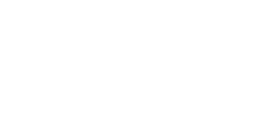
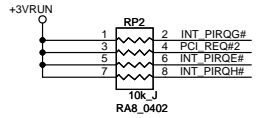
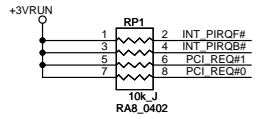
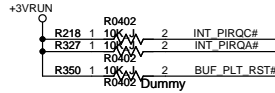
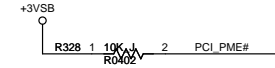


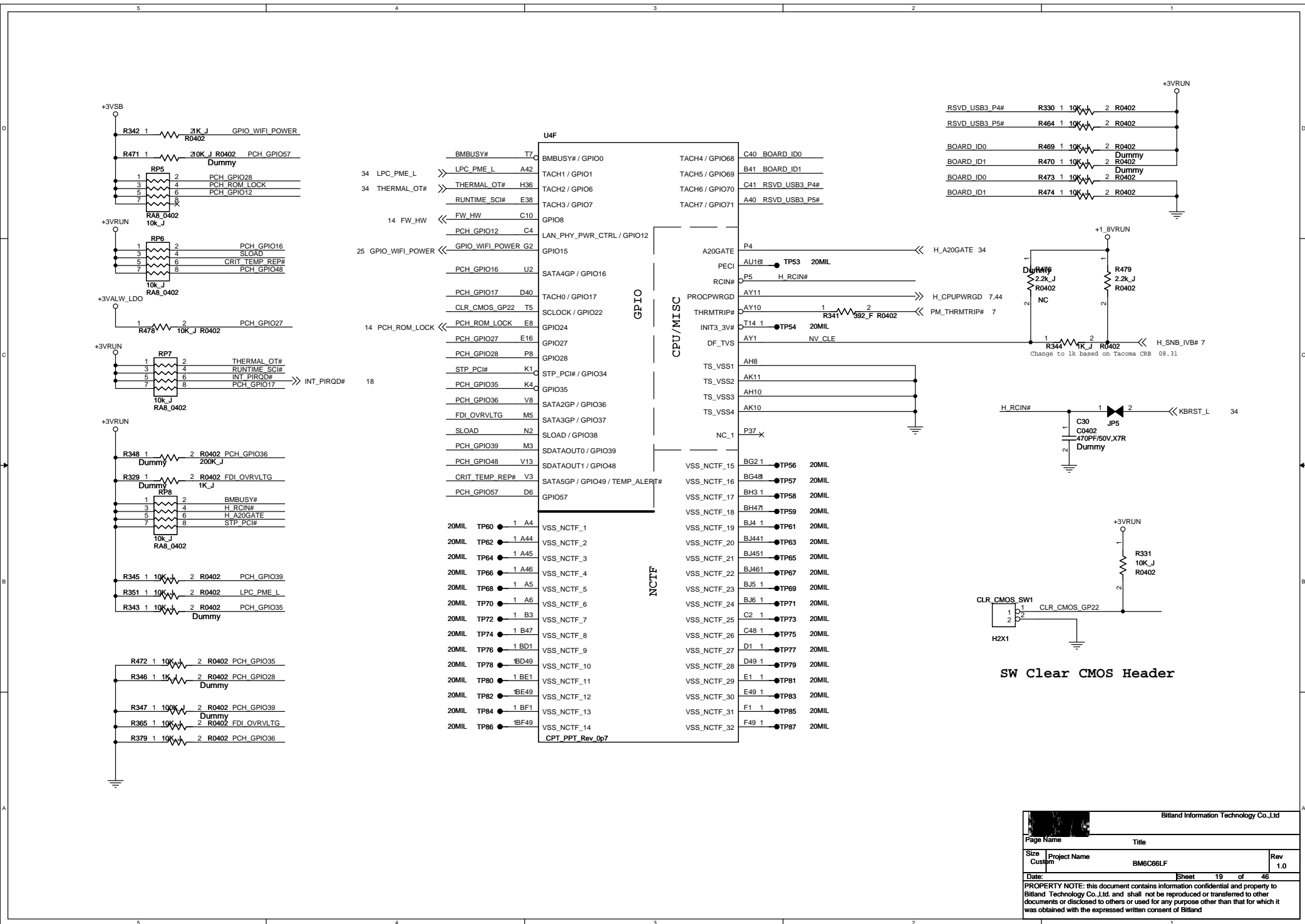
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Page Name		Title	
Size	Project Name	Rev	
Custom	BMSC68LF	1.0	
Date:		Sheet	16 of 46
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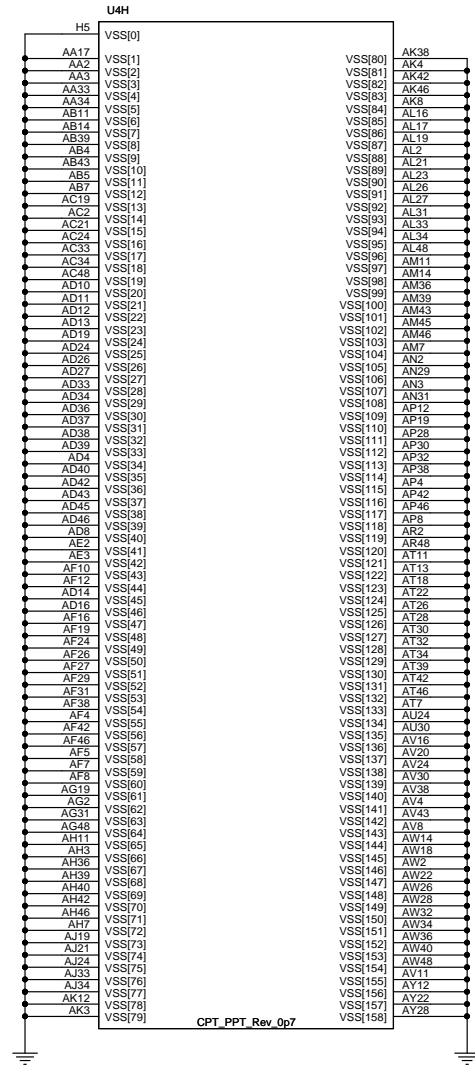
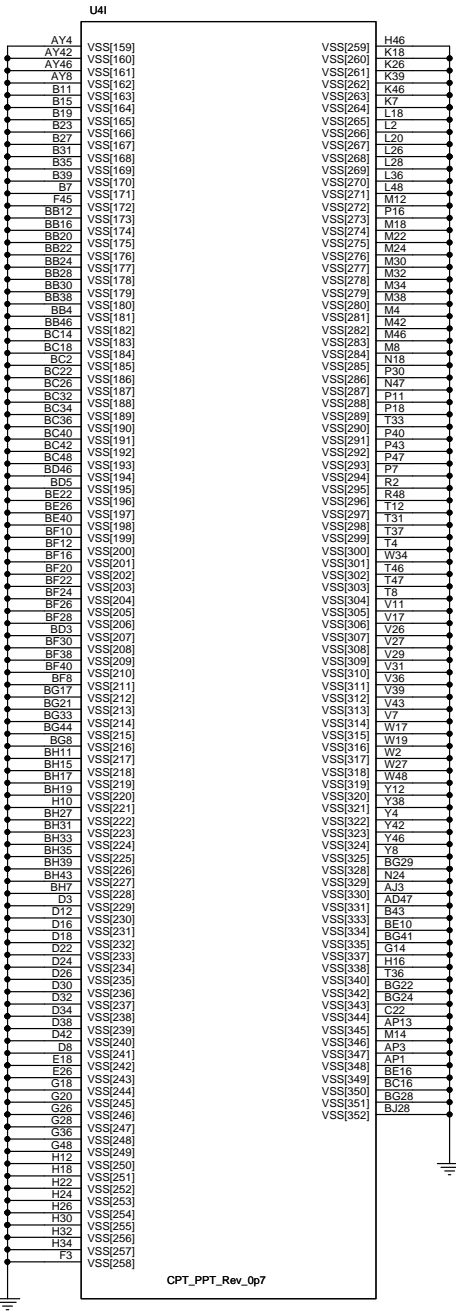


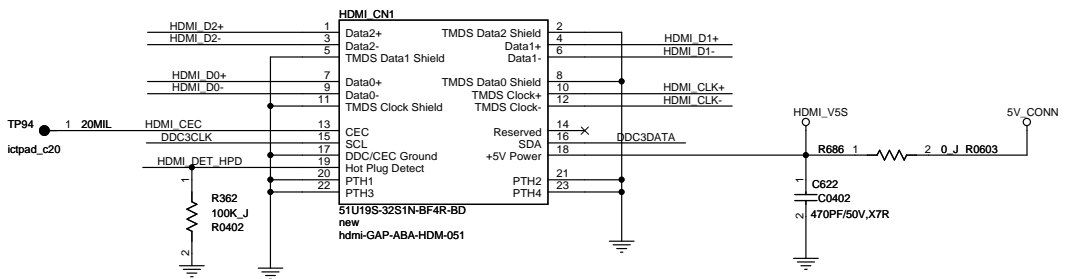
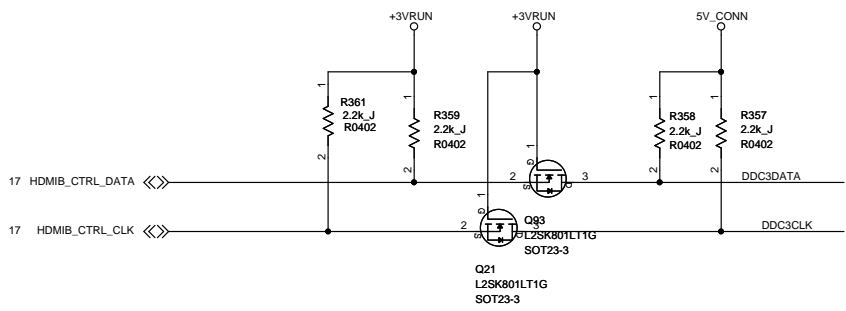
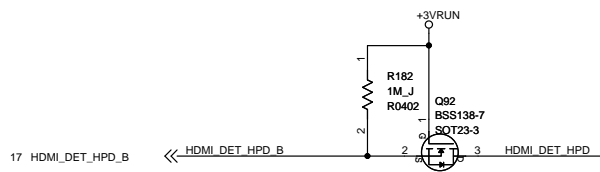
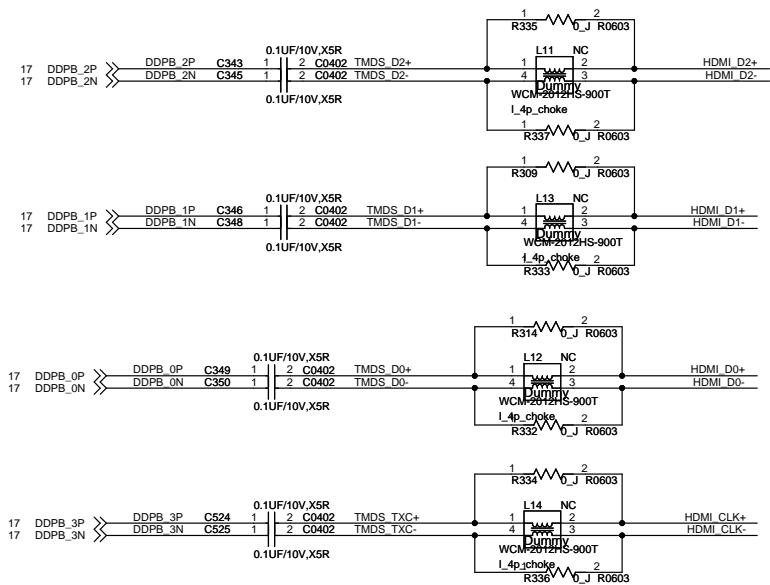
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Page Name		Title	
Size	Project Name	Rev	
Custom	BM6C66LF	1.0	
Date:		Sheet 17 of 46	
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USB3.0	HM76	HM70
Port1	ENABLE	ENABLE
Port2	ENABLE	ENABLE
Port3	ENABLE	DISABLED
Port4	ENABLE	DISABLED

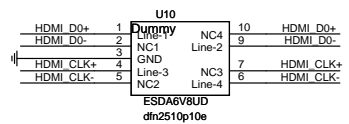




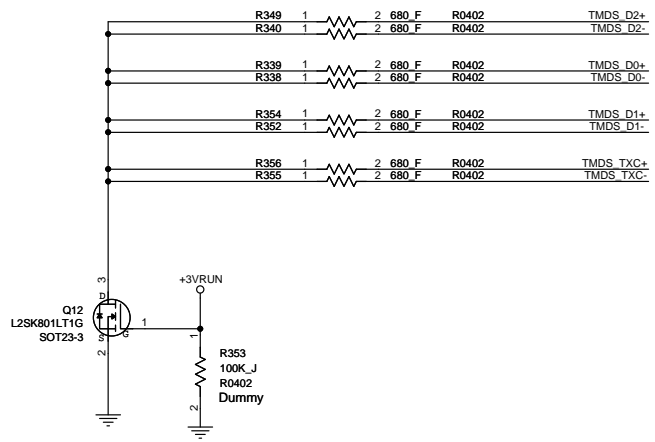
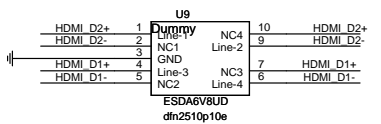


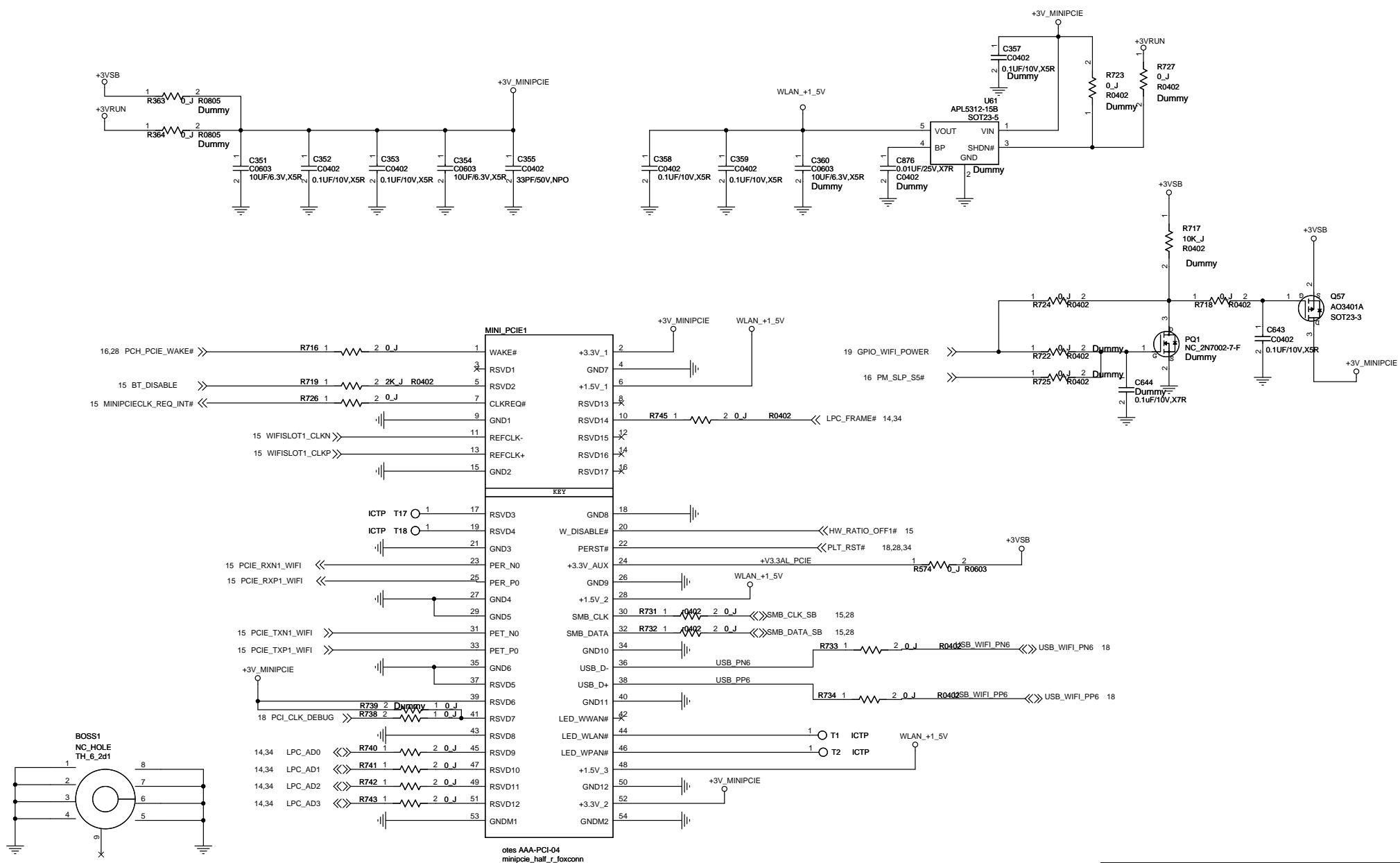


ESD

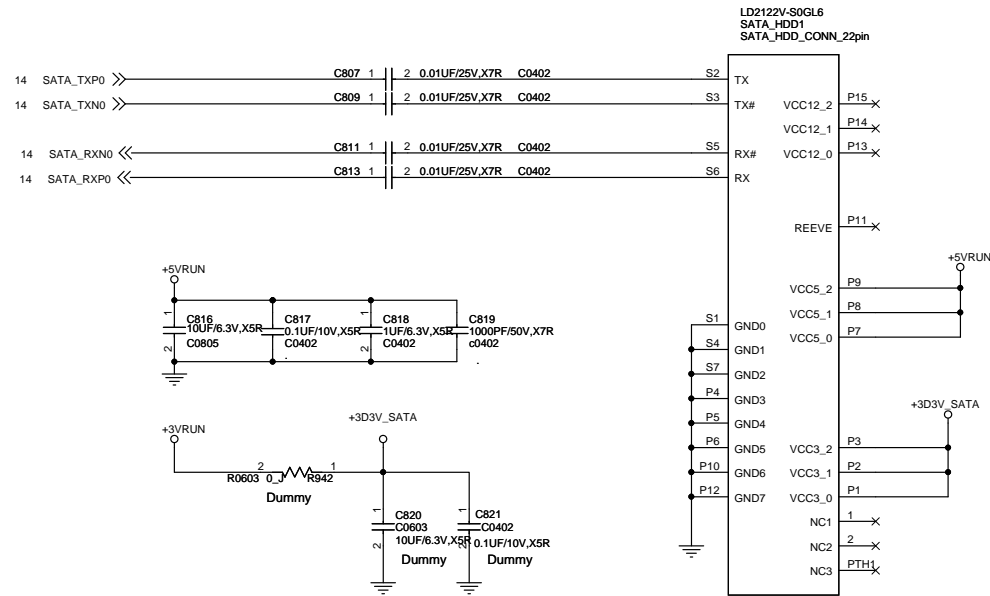


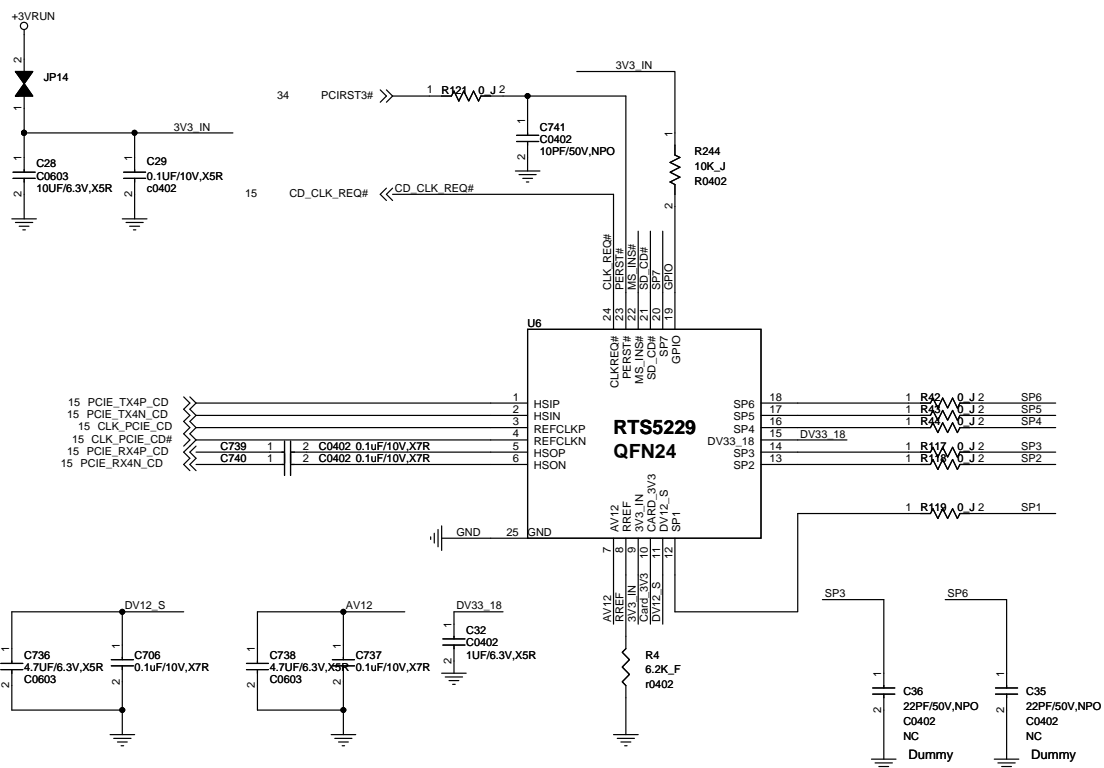
ESD





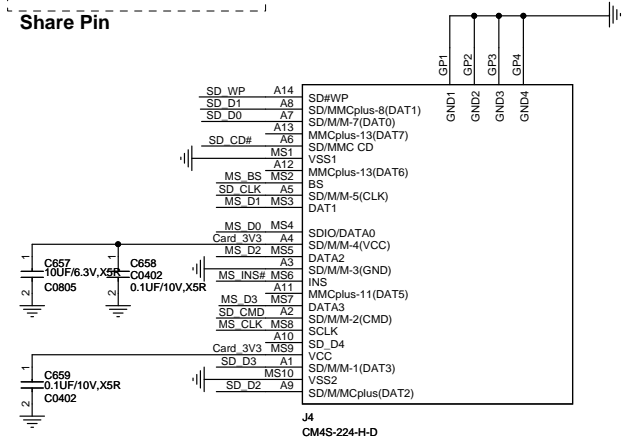
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Page Name	Title		
Size Custom	Project Name BM6C66LF	Rev 1.0	
Date:	Sheet	25	of 46
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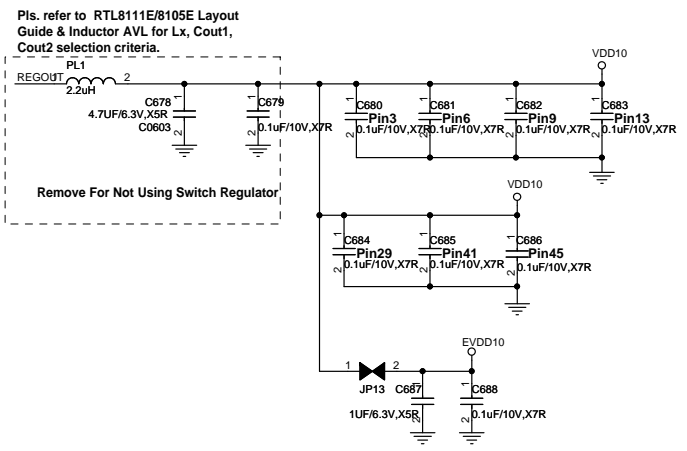
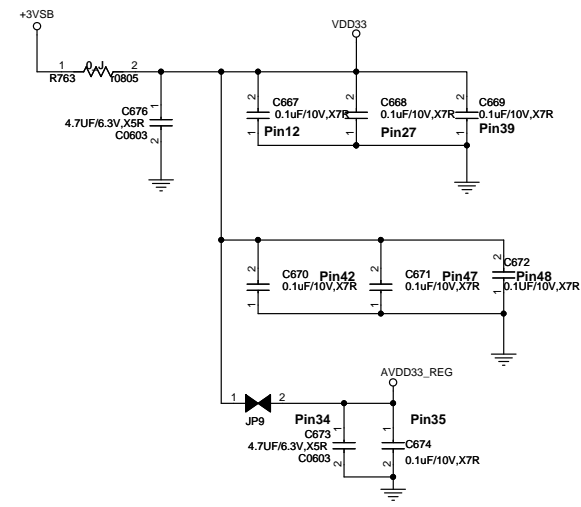
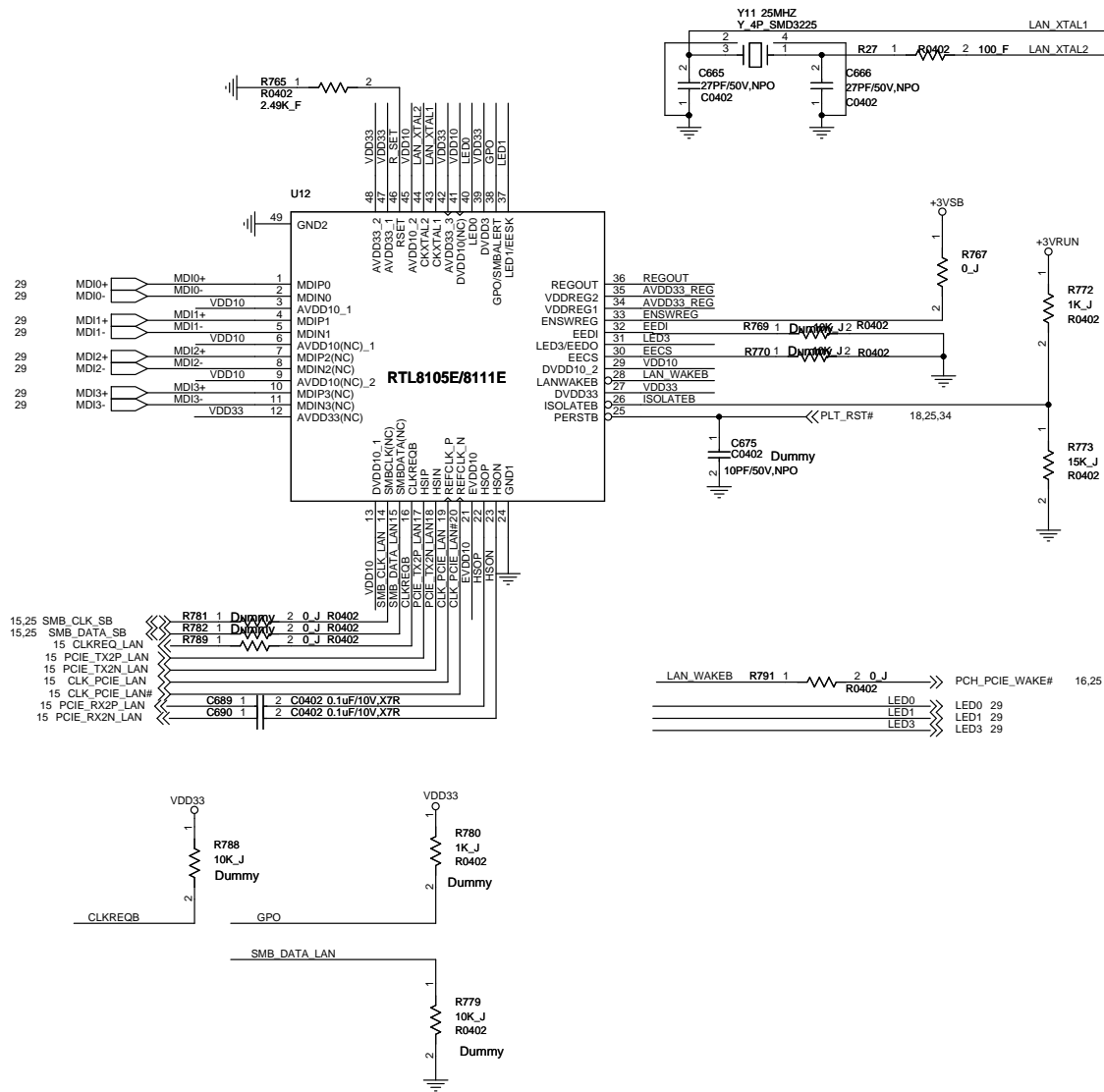


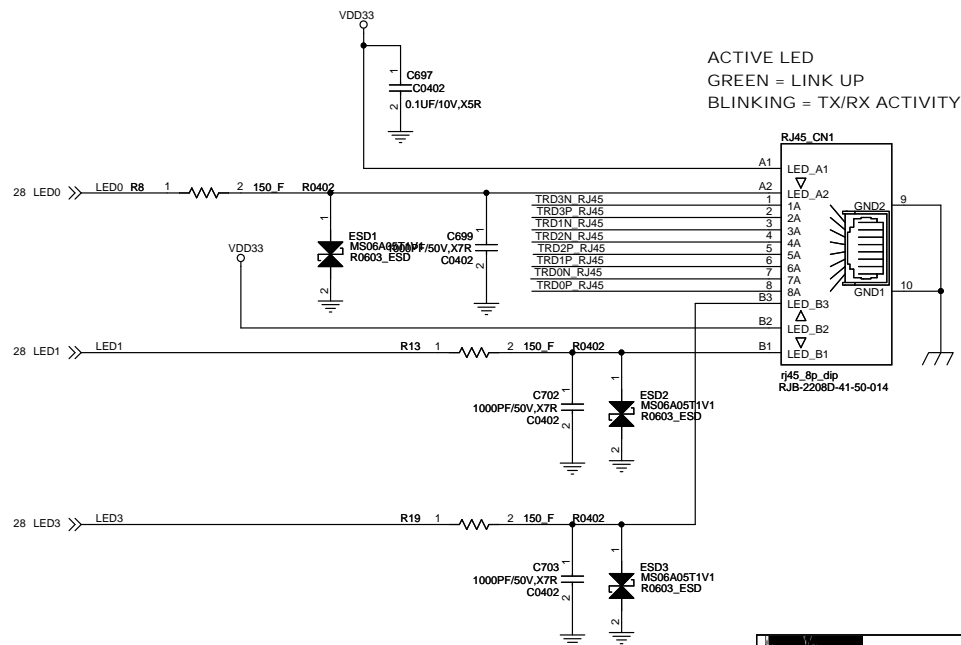
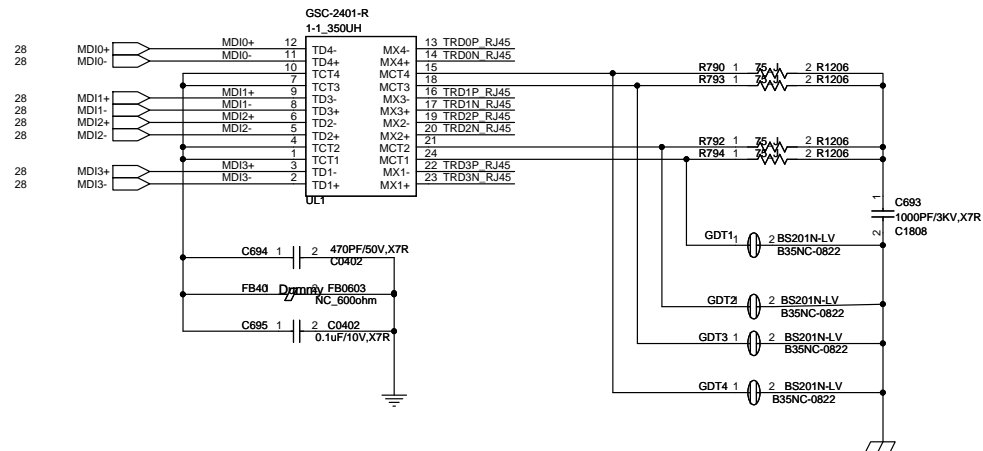
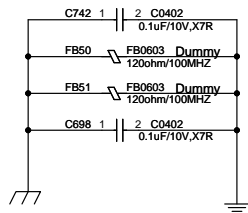
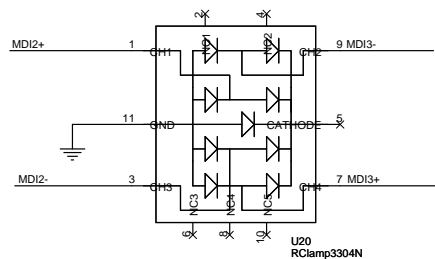
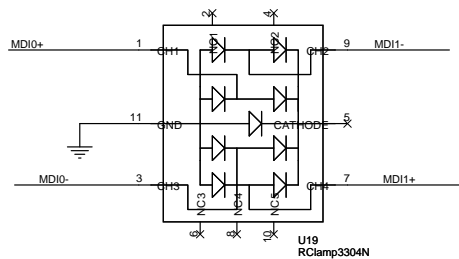


SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

SD4---???



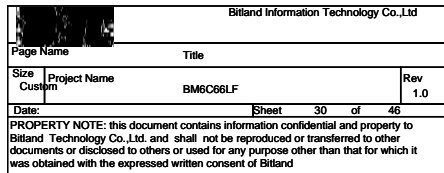


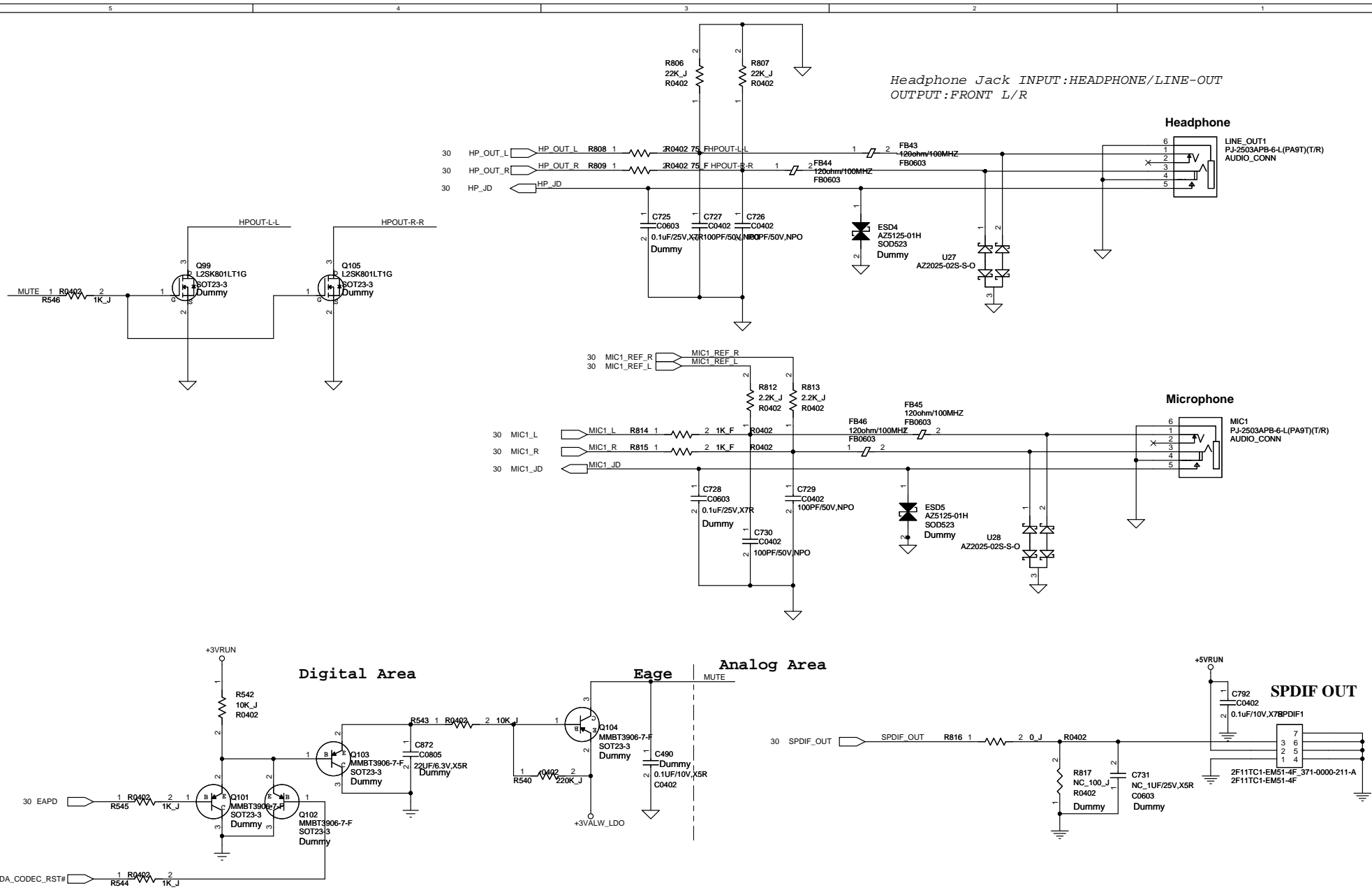



ACTIVE LED
GREEN = LINK UP
BLINKING = TX/RX ACTIVITY

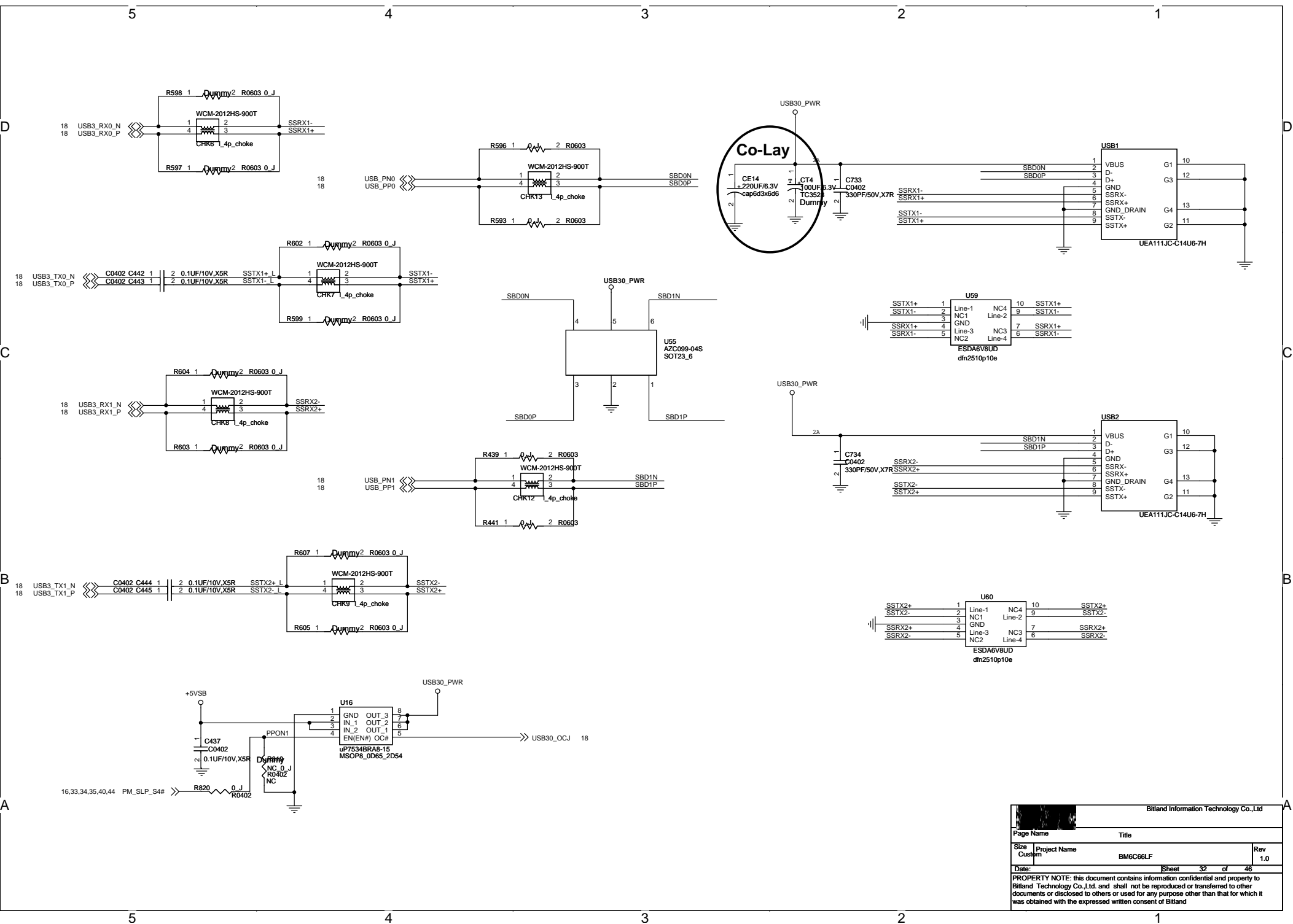
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Page Name	Title		
Size	Project Name	Rev	
Custom	BM6C66LF	1.0	
Date:	Sheet	29	of 46
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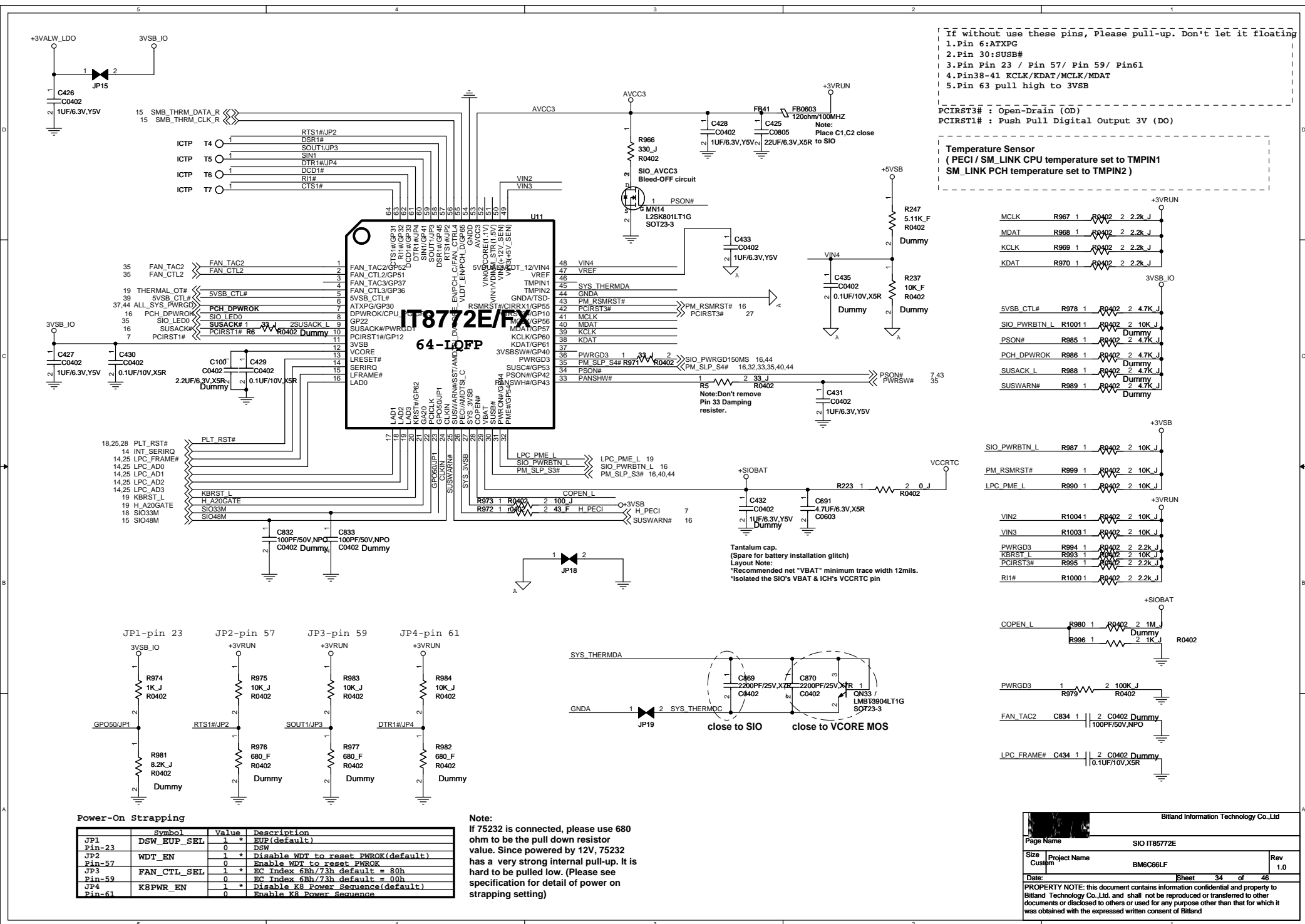
Layout Note:
All of JD resistors should be placed as close as possible to the sense pin of codec.



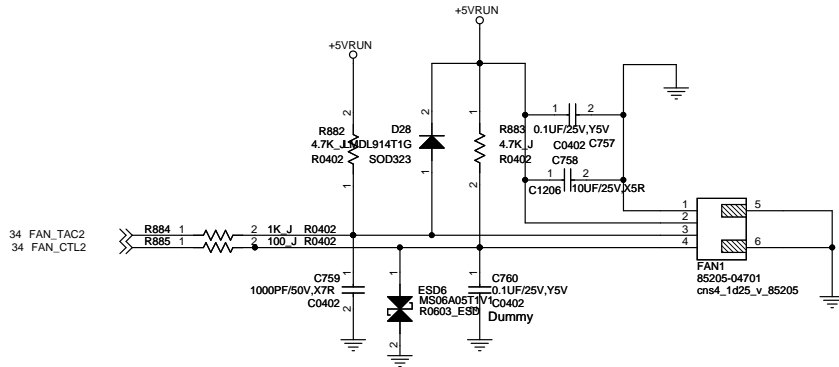


		Bitland Information Technology Co.,Ltd	
Page Name		Title	
Size	Project Name	Rev	
Custom	BM6C66LF	1.0	
Date:	Sheet 31 of 46		
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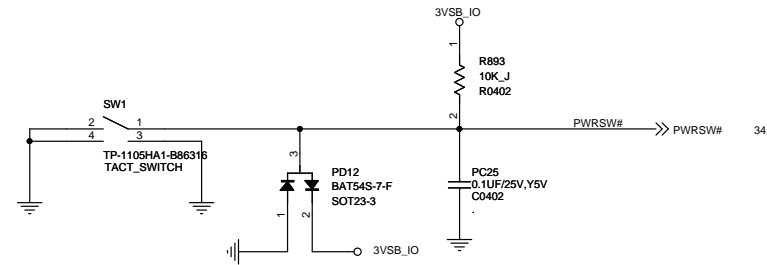




SYSTEM FAN

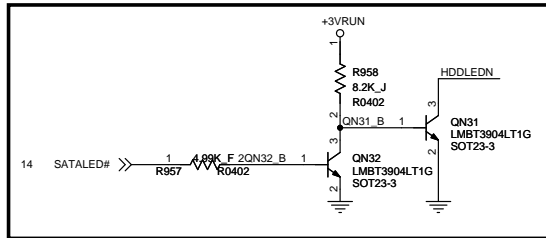
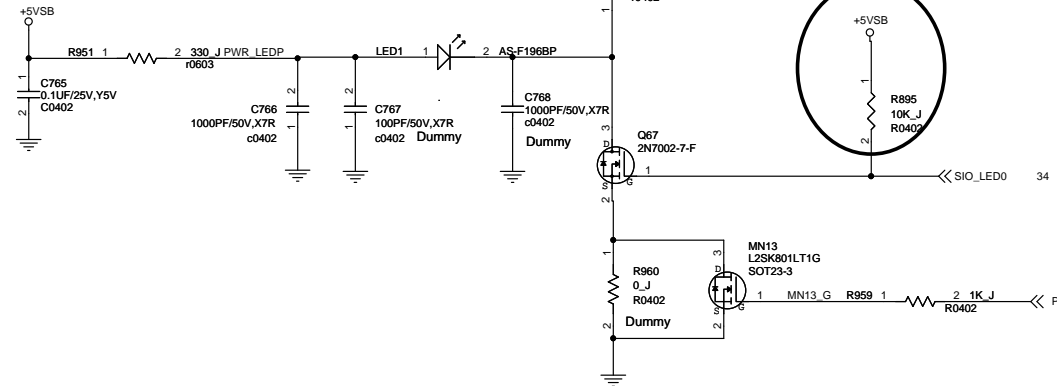
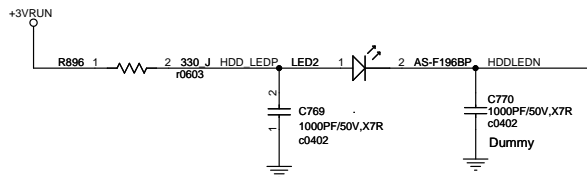


Power SW.



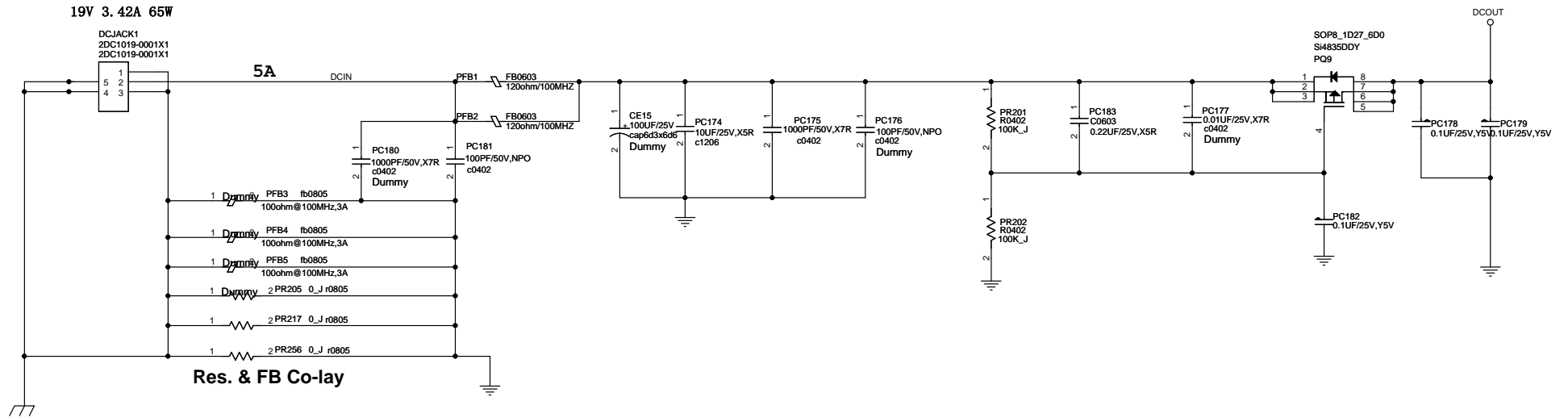
LED

Change to 470 for unify led light

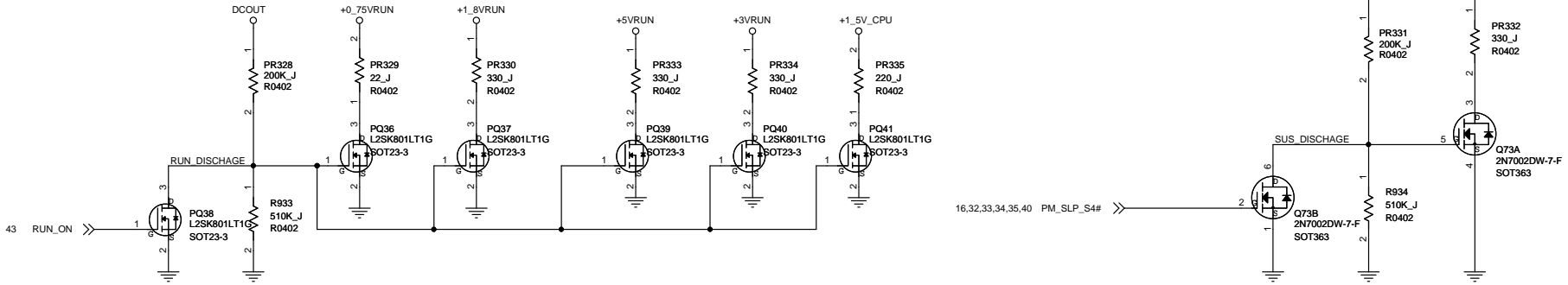


SATA LED Blink Once in Power On Issue

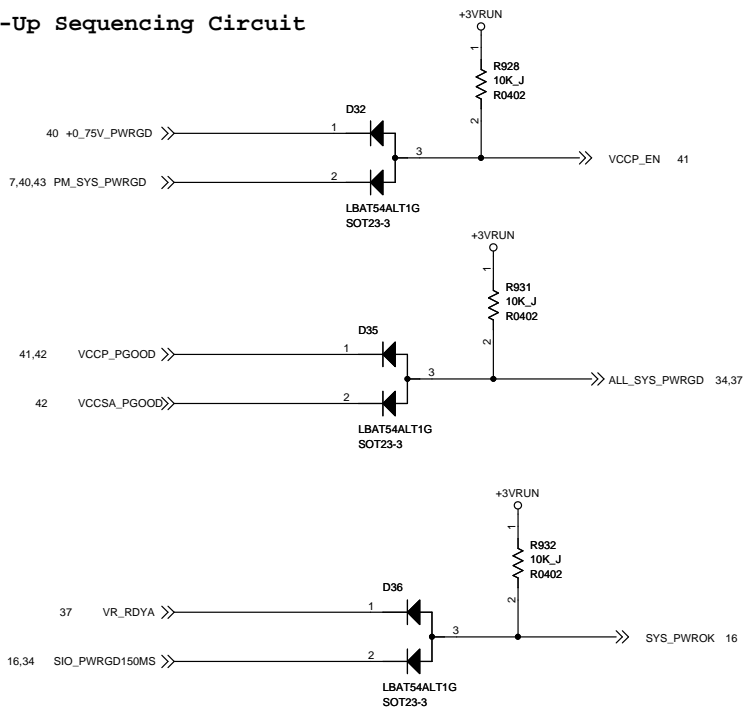
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Page Name	Title		
Size	Project Name	Rev	1.0
Custom	BM6C66LF		
Date:	Sheet	35	of 46
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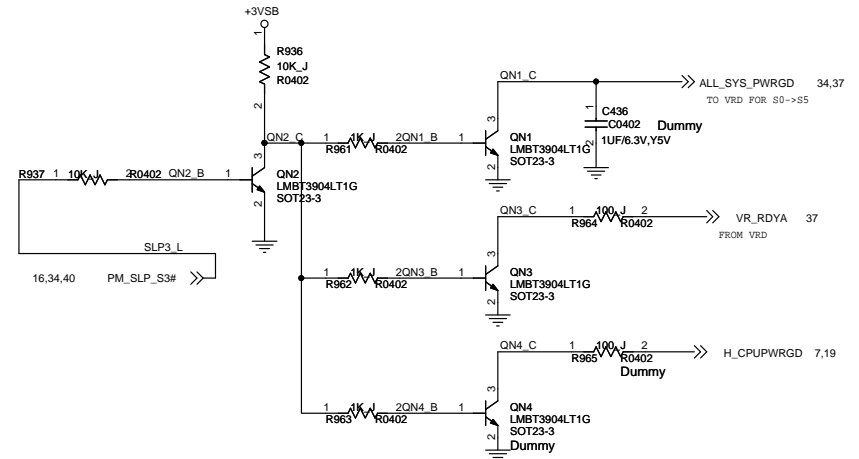
Power Discharge Circuit



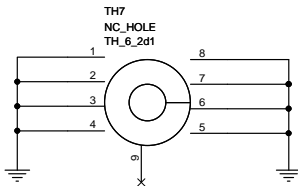
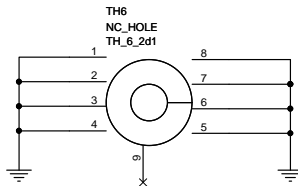
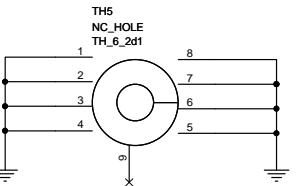
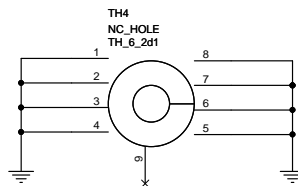
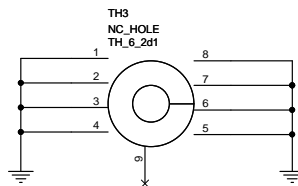
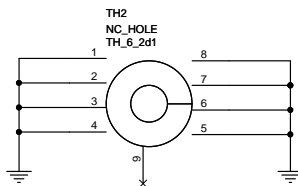
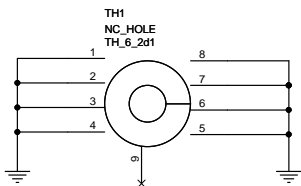
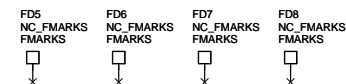
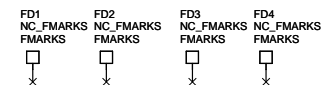
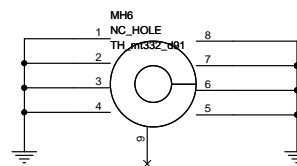
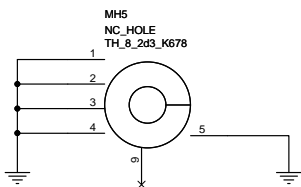
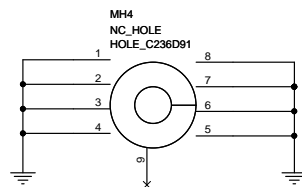
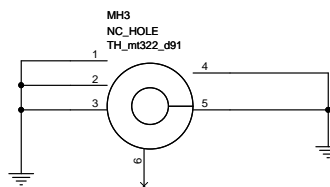
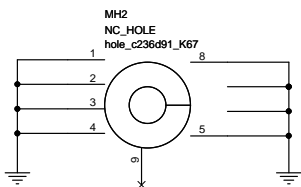
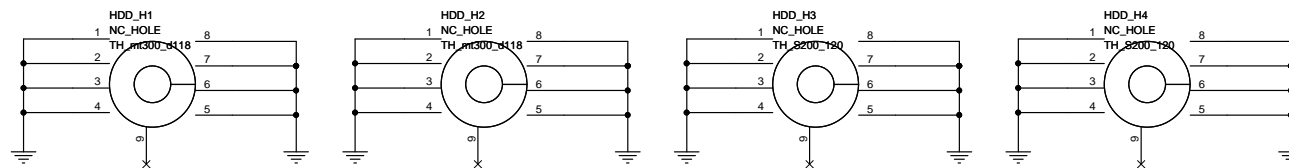
Power-Up Sequencing Circuit



Power Down Sequencing Circuit



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Page Name	Title		
Size	Project Name	Rev	1.0
Custom	BMSC68LF		
Date:	Sheet	44	of 46
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Page Name	HOLE/MARK		
Size Custom	Project Name BM6C66LF	Rev 1.0	
Date:	Sheet 45 of 46		
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REVISION HISTORY:

Rev	Date	Notes
V0.1	12/03/20	
V0.2	XX/XX/XX	